Novel Vedic Multiplication Technique and its Implementation – A Fast and Simple Method of Convolution

R. Bathija, Devesh Gupta, I. Suwalka

Abstract— Urdhya Triyakbhyam a new method of convolution based on Vedic Mathematics has been explained for digital signal processing. It has been shown that the convolution of large sequence can be found out in comparatively short time, by this method. We have demonstrated the capability of the method on eight samples. We had used Tanner tool for simulation and 16nm CMOS technology. A delay 53.21ns and power dissipation is 14.91uW has been found.

Index Terms— — Urdhya Triyakbhyam, Vedic Mathematics, CMOS technology, power dissipation, Convolution, Delay,VLSI implementation.

1 Introduction

With the latest advancement of VLSI technology the demand for portable and embedded digital signal processing (DSP) systems has increased considerably**.** Using programmable devices for DSP applications could narrow the gap between the flexibility of general purpose processor (GPP), programmable DSP (PDSP). FPGAs are being increasingly used for variety of computationally intensive applications. In digital signal processing convolution is a fundamental computation that is ubiquitous in many application areas [1].

Convolution is the most important and fundamental concept in signal processing and analysis. Many researchers have been trying to improve performance parameters of convolution system[ ]. One of the factors in performance evaluation of any system is speed. The core computing process in convolution is always a multiplication routine. Faster addition and multiplication are of extreme importance in DSP. Therefore, engineers are constantly looking for boosting performance parameters of it using new algorithms and hardware. After comparative study of different multipliers, Urdhva Tiryagbhyam sutra based on ancient Indian wisdom book – the Vedas, is shown to be an efficient multiplication algorithm [2][3].

2. Background: In Ref.[1],convolution is carried out by serial processing. They used only one 4×4 bit Vedic multiplier based on Urdhva Tiryagbhyam sutra. Though hardware is less, delay is more as sixteen multiplications are carried out one by one using only single multiplier. Direct method for calculating the linear convolution sum of two finite length sequences is easy to learn and perform. The approach is easy to learn because of the similarities to computing the multiplication of two numbers by a pencil and paper calculation.

FPGA implementation is future work [2]. In parallel FIR filter algorithm, the preprocessing, post-processing and sub-filter matrices can be calculated easily with Matlab. Then, Matlab can be used to automatically generate Verilog code for the hardware implementation of this algorithm [5]. But in automatically generated code there is no control on architecture level.

ROM look up tables can be used to implement the computational modules. Multipliers can be realized using memory based approach. Multiplication of two n bit input variables can be performed by ROM table of size 2 with power 2n entries [7]. But this approach is not efficient in area point of view.CRT algorithm minimizes multiplication operation at cost of increase in addition operations [8]. Parallel implementation improves speed [9]. The sutras in Vedic mathematics are easy to understand, easy to apply and easy to remember. Vedic maths is helpful to software developers as it is more scientific than the normal system of mathematics [10].

3. Convolution: Discrete time convolution can be defined as $y[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k]$

Where x[n] is the input and h[n] is the impulse response. Thus the output of the LTI system is given by a weighted sum of time shifted impulse responses. It is known as convolution sum and represented as *. Thus $x[n] * h[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k]$

For example if

then convolution sum will be calculated as

For example $x[n] = \{10,20,30,40\}$ & $h[n] = \{2,3,5,6\}$

Then

Similarly in the case of binary

In above method of linear convolution, it is simply a multiplication process with addition with no carry being propagated. This method utilizes large area of the chip. Also this method is bit slow & slower if we take large no of samples for convolution.

4. Proposed method of convolution:

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications.

The work presented here, makes use of Vedic Mathematics. “Urdhva Tiryagbhyam Sutra” or “Vertically and Crosswise Algorithm” of Vedic

- *R. Bathija currently working as associate professor in Electronics and Communication Engineering department at JECRC, Jaipur. E-mail: rajesh.ece@jecrc.ac.in*
- *Devesh Gupta is currently working as assistant professor in Electronics and Communication Engineering department at JECRC, Jaipur, India.*
- *I. Suwalka is currently working as assistant professor in Electronics and Communication Engineering department at CTAE, MPUAT, Udaipur, India*

mathematics for multiplication is used to develop digital multiplier architecture. This looks quite similar to the popular array multiplier architecture. This Sutra shows how to handle multiplication of a larger number (N x N, of N bits each) by breaking it into smaller numbers of size (N/2 = n, say) and these smaller numbers can again be broken into smaller numbers (n/2 each) till we reach multiplicand size of (2 x 2) .Thus, simplifying the whole multiplication process.

Let number1 = (10)2 and number2 = (10)2. Multiplication of these numbers, using Urdhva Tiryagbhyam is shown in fig. 1.

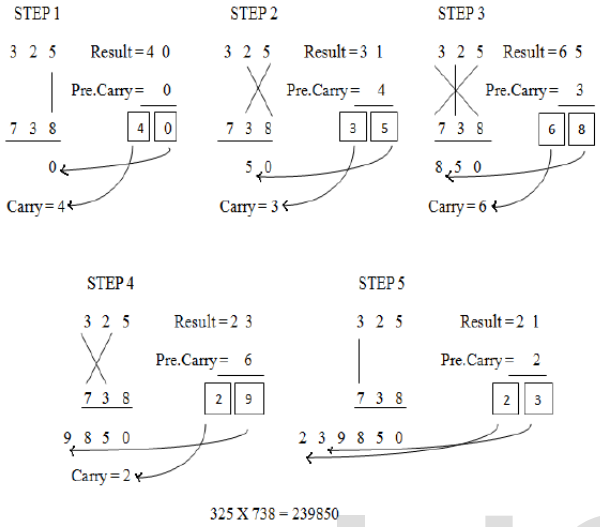

Fig.1 Multiplication of two decimal numbers by Urdhava Tiryakbhyam Sutra [1]

Now we can use novel method of long multiplier using smaller multiplication as explained in [2].

For reference 2x2 multiplier is shown in fig 2 and 4x4 multiplier using 2x2 multiplier is shown in fig 3.

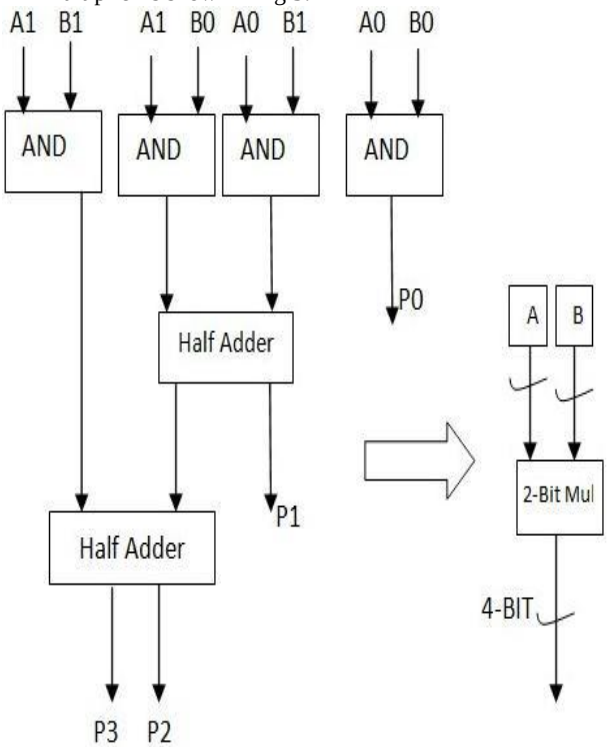

Fig. 2 2x2 bit multiplier using Urdhva Tiryagbhyam Sutra [1]

Same approach is used for convolution also. For example if $x[n] = \{a3, a2, a1, a0\}$ & $h[n] = \{b3, b2, b1, b0\}$ then the convolution of these we can make simpler by taking 2 sample at a time and calculating the convolution simultaneously so that speed will be faster. Then we add the appropriately.

The method is illustrated as below.

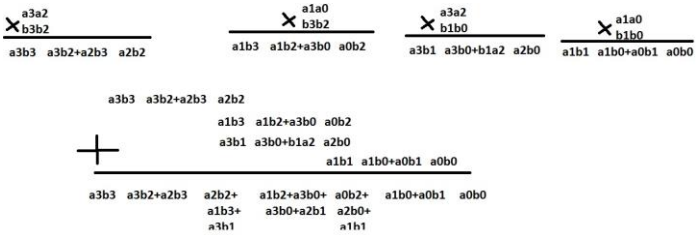

Figure 3. proposed method of convolution of 4x4

So using this method let us do above convolution of $x[n] = \{10,20,30,40\}$ & $h[n] = \{2,3,5,6\}$

10 20 | 10 20 | 30 40 | 30 40

2 3 | 5 6 | 2 3 | 5 6

20, 30+40, 120 | 50, 60+100, 120 | 60, 90+80, 240 | 150,180+200, 60

20 70 60
50 160 120
60 170 120
150 380 240

20 70 190 330 390 380 240

Same method can be extended to any high value. For example 8x8 convolution can be implemented by 4*4 convolution as follows

$x[n] = \{2,3,4,5,6,7,8,9\}$, & $h[n] = \{1,0,4,5,2,3,6,7\}$

2,3,4,5 | 2,3,4,5 | 6,7,8,9 | 6,7,8,9

1,0,4,5 | 2,3,6,7 | 1,0,4,5 | 2,3,6,7

2,3,12,27, 31,40,25 | 4,12,29,55, 60,58,35 | 6,7,32,67, 67,76,45 | 12,32,73,126, 124,110,63

2 3 12 27 31 40 25
4 12 29 55 60 58 35
4 7 32 67 67 76 45
12 32 73 126 124 110 63

2,3,12, 27, 39, 59, 86,122,139,166, 153, 126, 124, 110, 63

6. Conclusion: A circuit of high speed and low power can be designed on the basis Urdhava Tiryakbhyam sutra. The convolutions can be carried out with the new design using short sample convolutions. Present method has advantage over the existing methods in terms of i) low power; ii) high speed; iii) small area and iv) less no of MOSFETs required. The circuit will help to build the high speed & low power DSP processor. The circuit also has scope to identify the n=0, point if it is not the starting point in x[n] & h[n].

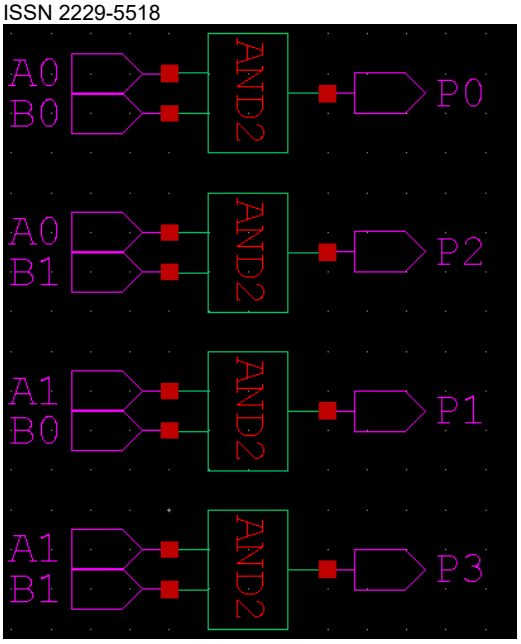

Fig. 4 2x2 convolution

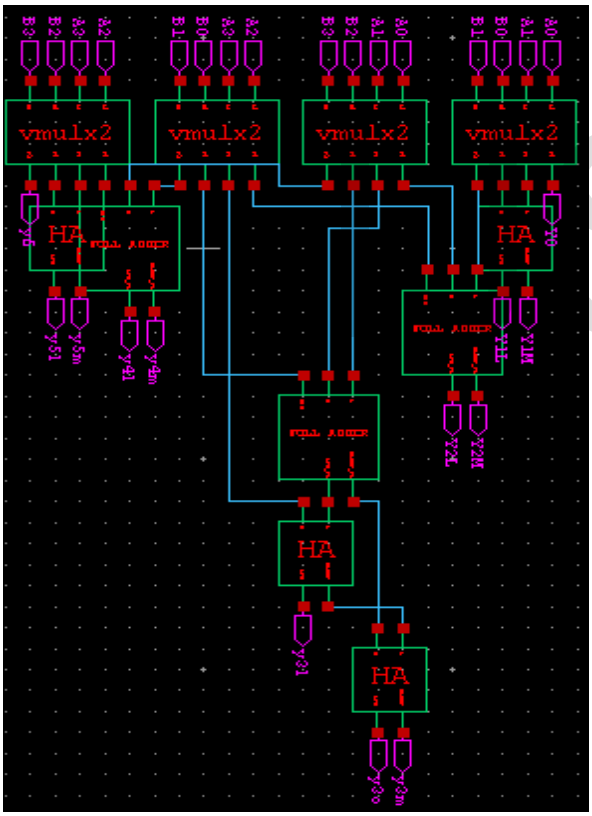

Fig. 5 4x4 convolution using 2x2 convolution vmulx2

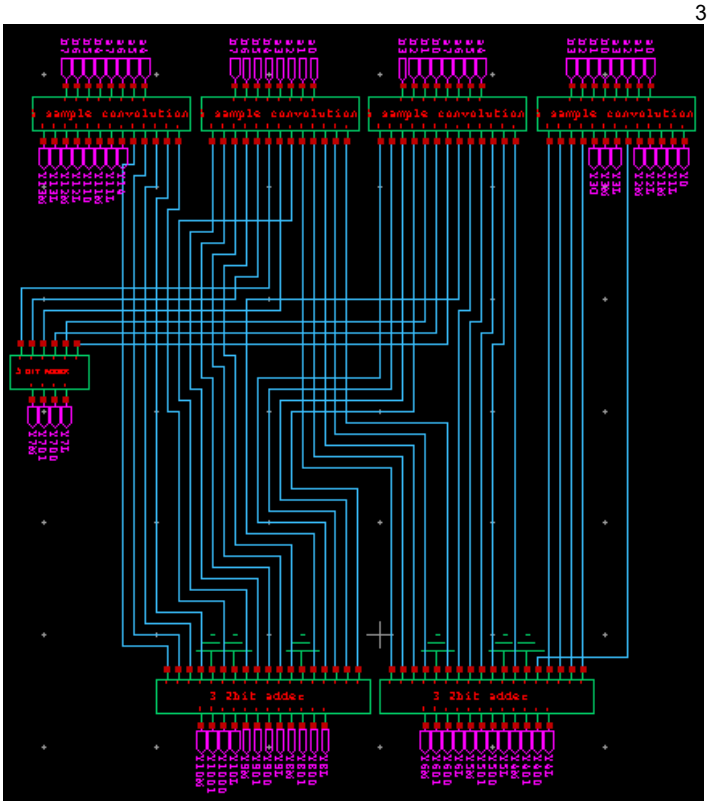

Fig 6 8x8 convolution using 4x4 convolution

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